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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Mamoru NAKASUJI, et al.

ATTN: Box Missing Parts

Serial No.: 09/891,611

Group Art Unit: Unknown

Filed: June 27, 2001

Examiner: Unknown

For: INSPECTION SYSTEM BY CHARGED PARTICLE BEAM AND METHOD OF
MANUFACTURING DEVICES USING THE SYSTEM

10/24/2001 SDIRETA1 00000083 09891611

01 FC:103
02 FC:102
03 FC:104

2592.00 OP
3528.00 OP
280.00 OP

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Date: October 22, 2001

Sir:

Prior to calculation of the filing fee and examination of this application, please amend the
above-identified application as follows:

IN THE CLAIMS:

Please amend claims 53, 55, 75 and 81 as follows:

53. (Amended) The inspection apparatus of claim 51 or 52 wherein the apparatus
is constructed so that an energizing condition of an objective lens is obtained under a state where
a pattern on a wafer is electrically charged.

55. (Amended) A method for manufacturing semiconductor devices wherein a wafer
during a manufacturing process or after processing is evaluated by using the inspection apparatus
of any one of claims 51, 52 or 54.

75. (Amended) A method for manufacturing semiconductors by using the inspection apparatus of claim 71 or 72.

81. (Amended) A device manufacturing method for evaluating a wafer during manufacturing process by using the inspection apparatus of any one of claims 77 to 79.

Please add new claims 101-104 as follows:

101. (New) A method for manufacturing semiconductor devices wherein a wafer during a manufacturing process or after processing is evaluated by using the inspection apparatus of claim 53.

102. (New) A method for manufacturing semiconductors by using the inspection apparatus of claim 73.

103. (New) A method for manufacturing semiconductors by using the inspection apparatus of claim 74.

104. (New) A device manufacturing method for evaluating a wafer during manufacturing process by using the inspection apparatus of claim 80.

09/891,611-102201

Applicants: Mamoru NAKASUJI, et al.
Serial No.: 09/891,611

Docket No.: 010817
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REMARKS

Claims 53, 55, 75 and 81 have been amended. Claims 101-104 have been added. Claims 1-104 are pending.

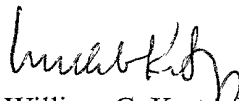
A marked-up version of the changes made to the claims is enclosed herewith as "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

The above amendments to the claims have been made to correct the multiple dependency of claims 55, 75 and 81. It is noted that the enclosed Certified English Translation of the present application contains a typographical error in claim 53. Corrective thereto, the dependency of said claim as been changed to reflect the originally filed Japanese text version of the same. Further, new claims 101-104 have been added to include the subject matter deleted by the current amendment. It is respectfully submitted that purpose of the amendments incorporated herein are to better place the application in condition for examination.

In the event that any additional fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI
McLELAND & NAUGHTON, LLP

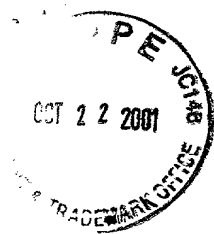


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Enclosures: Version With Markings to Show Changes Made
Amendment Transmittal (w/ appropriate fees)

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Q:\FLOATERS\WGK\010817 Preliminary Amendment



VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. Serial No. 09/891,611

IN THE CLAIMS:

Claims 53, 55, 75 and 81 have been amended as follows:

53. (Amended) The inspection apparatus of claim ~~52~~ 51 or 52 wherein the apparatus is constructed so that an energizing condition of an objective lens is obtained under a state where a pattern on a wafer is electrically charged.

55. (Amended) A method for manufacturing semiconductor devices wherein a wafer during a manufacturing process or after processing is evaluated by using the inspection apparatus of any one of claims ~~51-54~~ 51, 52 or 54.

75. (Amended) A method for manufacturing semiconductors by using the inspection apparatus of ~~any one of claims 71 to 74~~ claim 71 or 72.

81. (Amended) A device manufacturing method for evaluating a wafer during manufacturing process by using the inspection apparatus of any one of claims 77 to ~~80~~ 79.